ABSTRACT

An interface to transfer data between a memory control hub and an input/output control hub of a chipset within a computer system. One embodiment of the interface includes a bi-directional data signal path and a pair of source synchronous strobe signals. The data signal path transmits data in packets via split transactions. In addition, the packets include a request packet and a completion packet, if necessary. Furthermore, in one embodiment, the request packets include a transaction descriptor.